

002090" E2498560

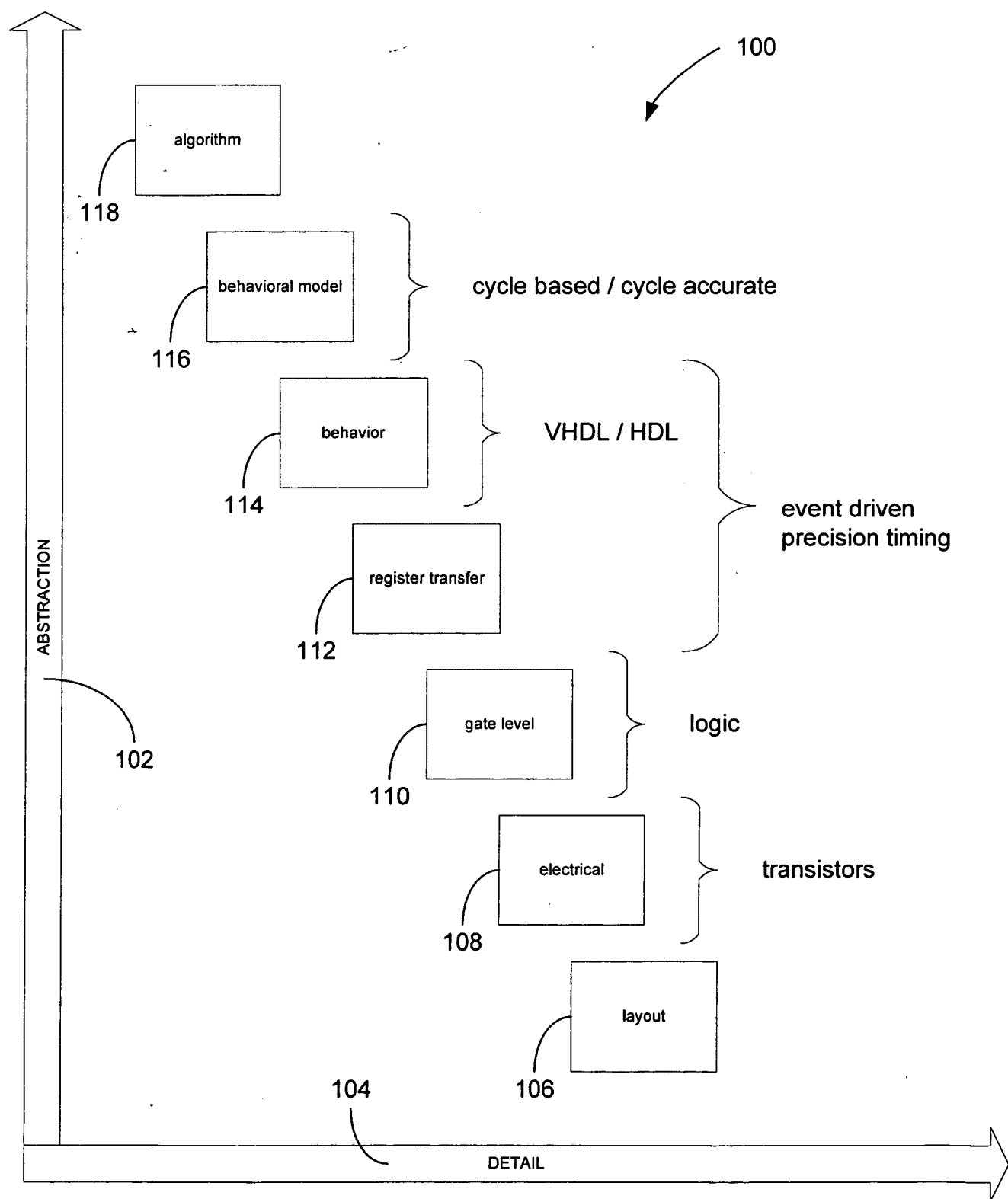


FIG. 1

002090-22493560

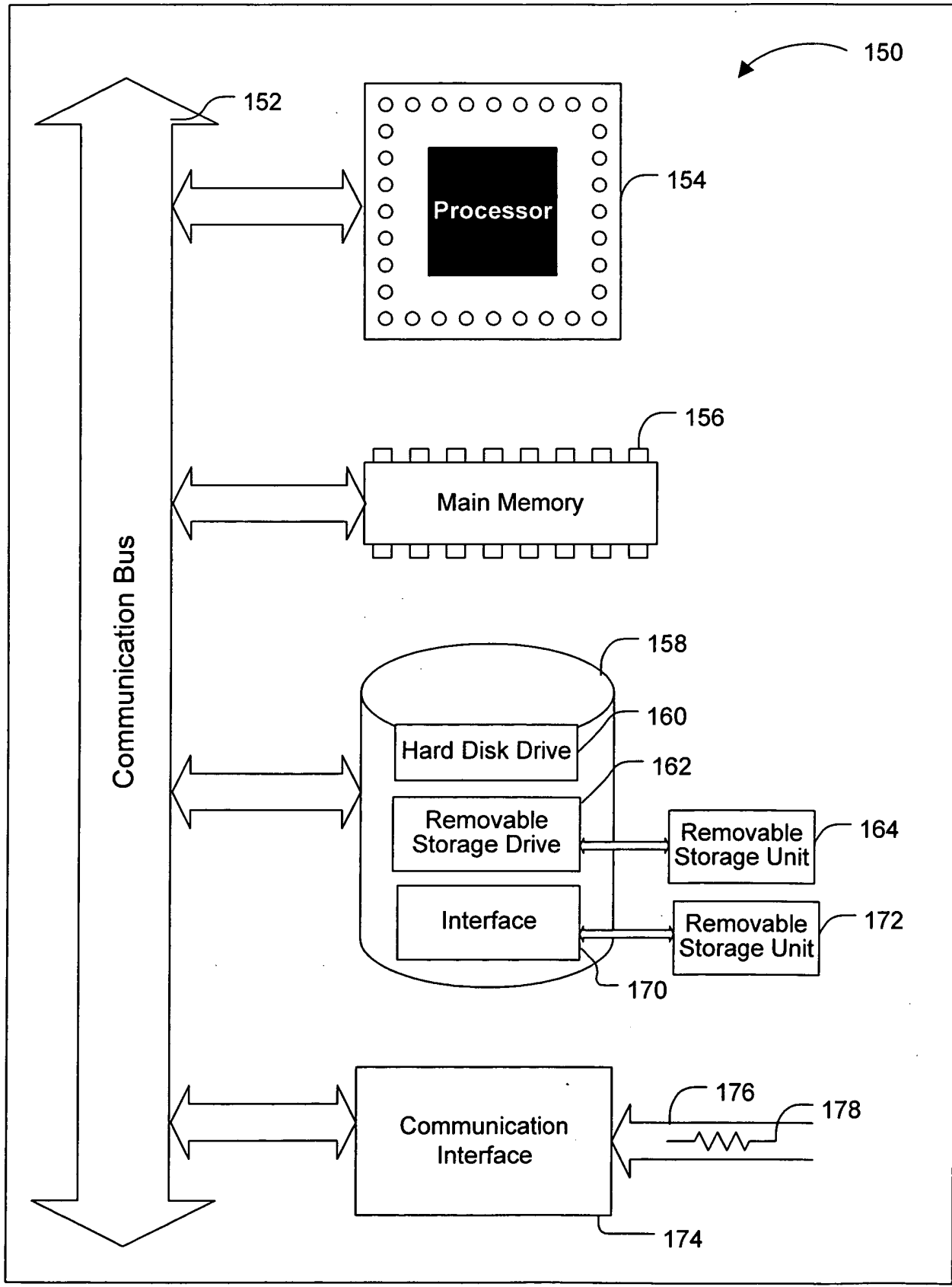


Fig. 1A

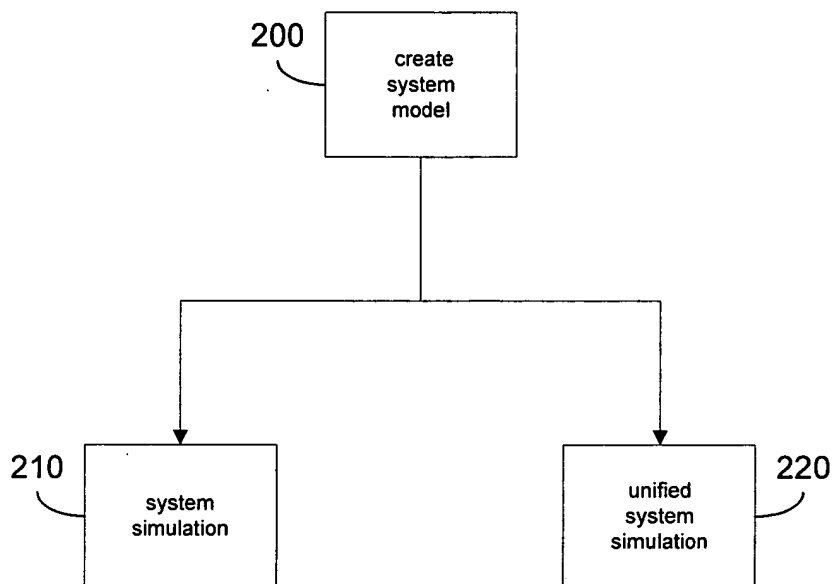


FIG. 2

002090" 22192560

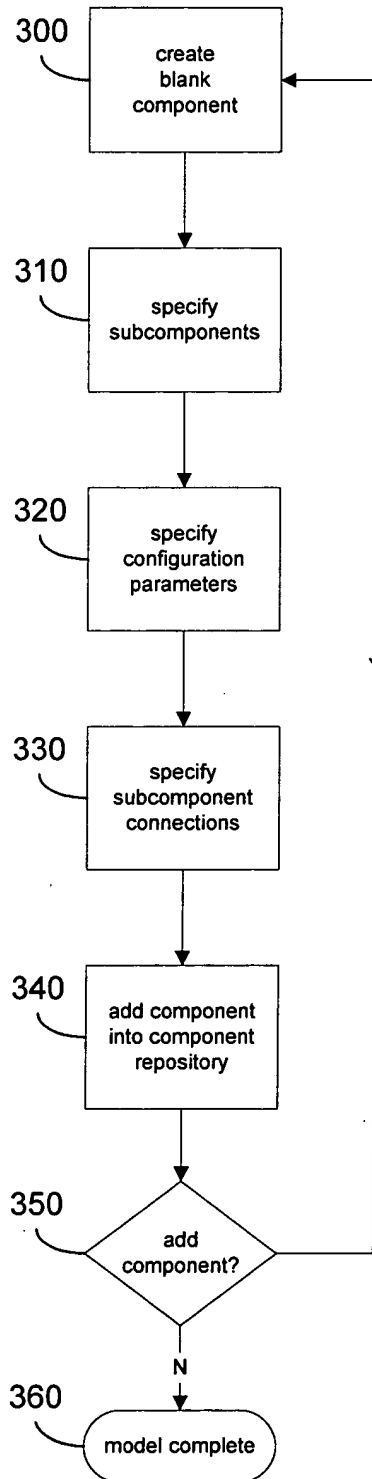


FIG. 3

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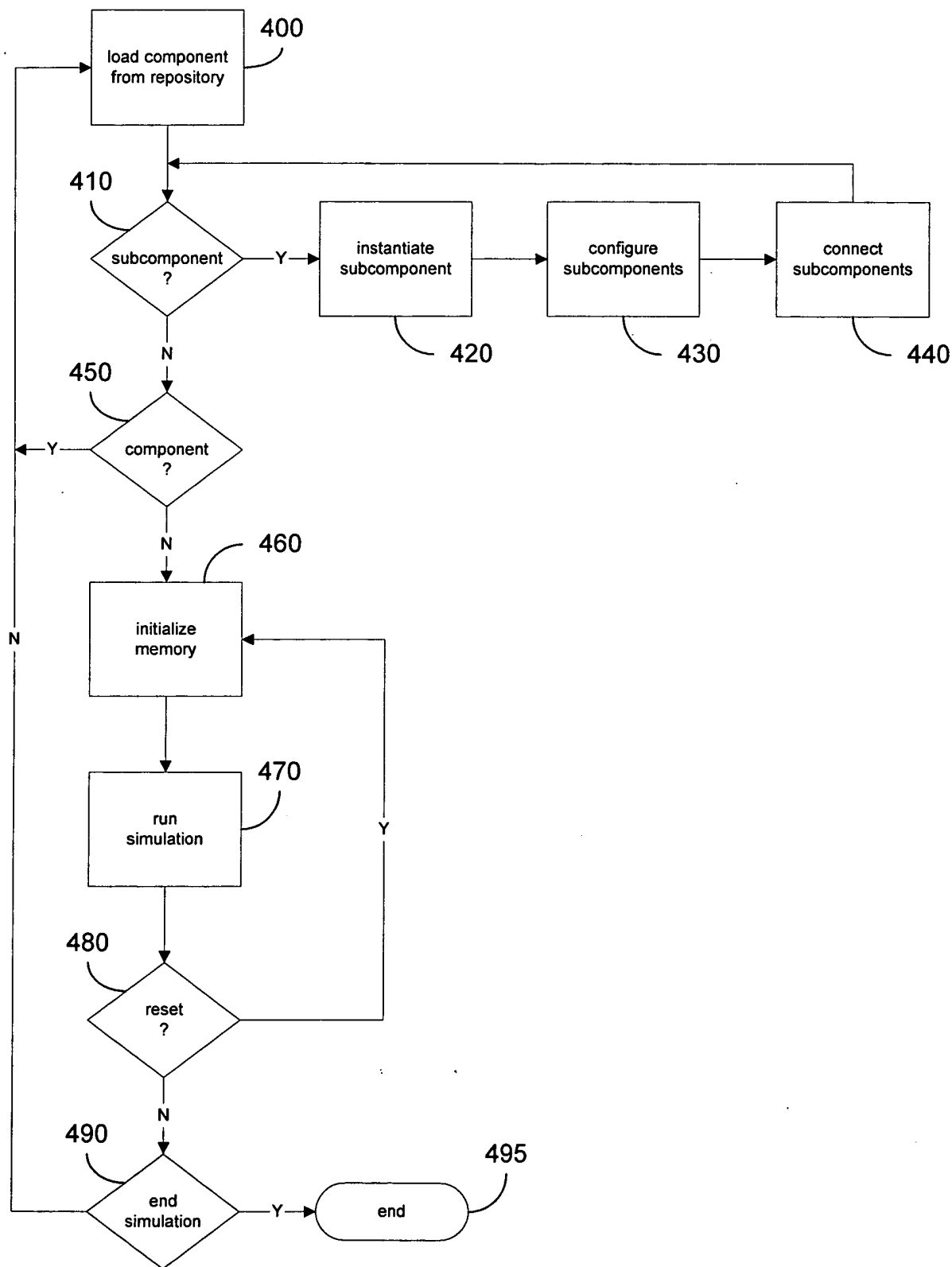


FIG. 4

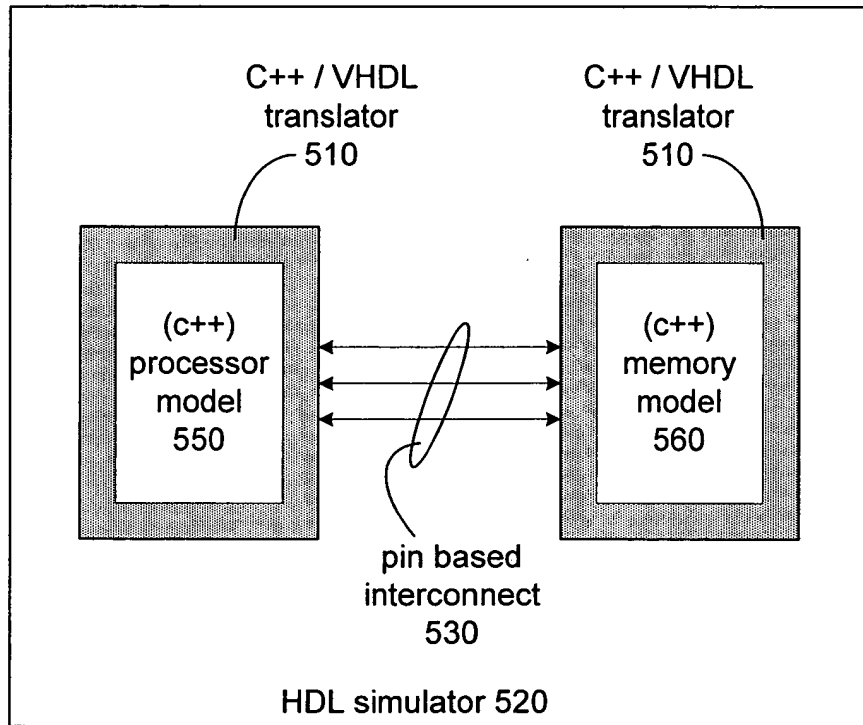


FIG. 5

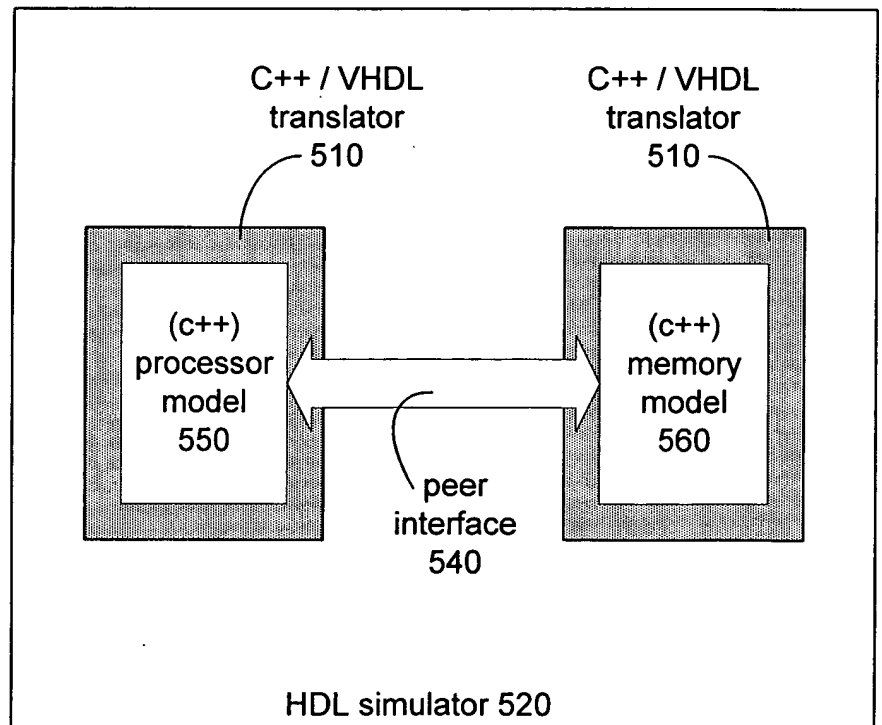


FIG. 5A

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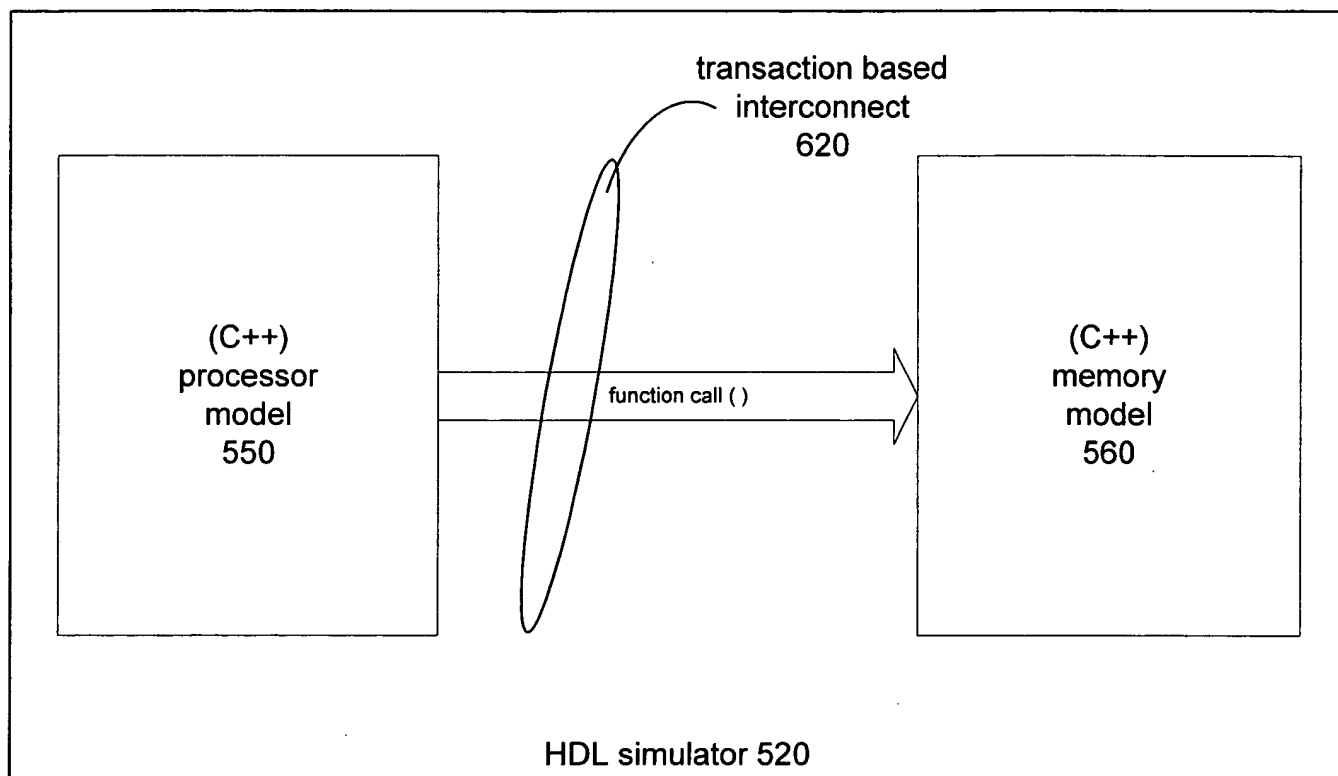


FIG. 6

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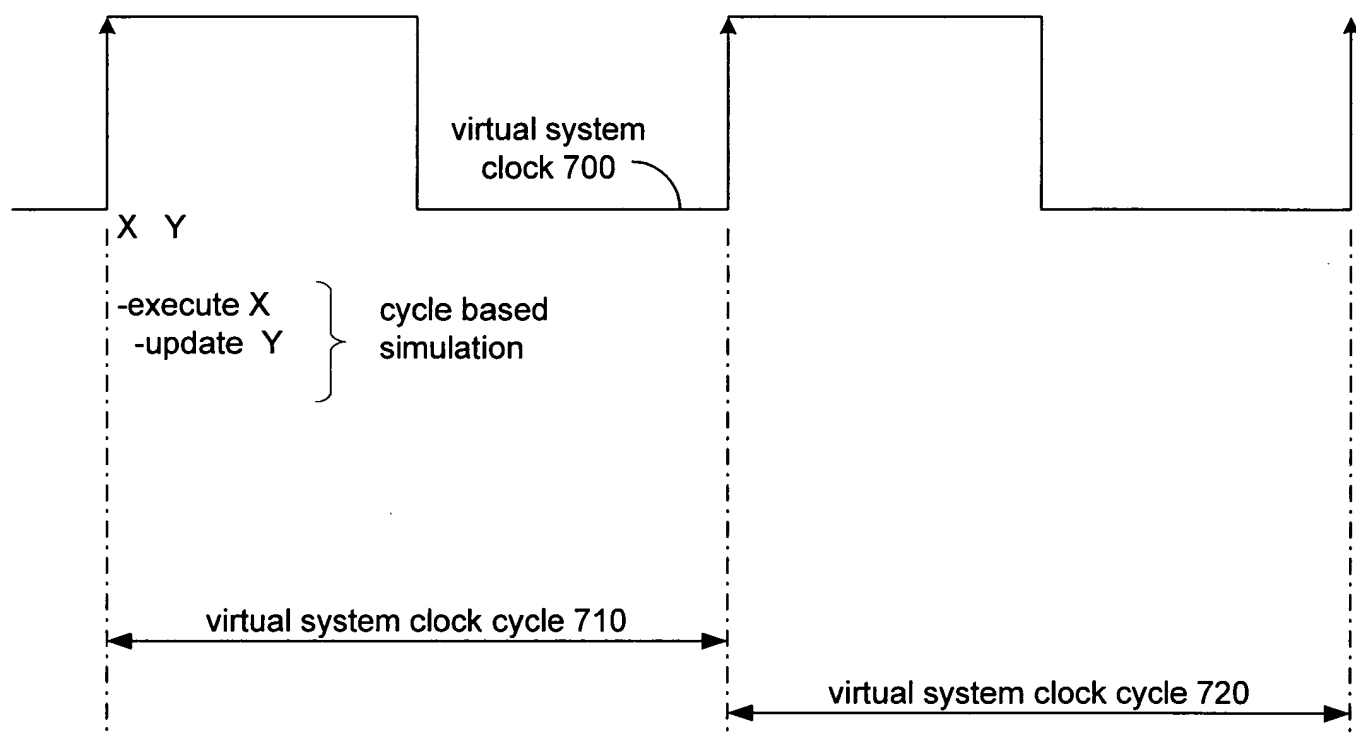


FIG. 7

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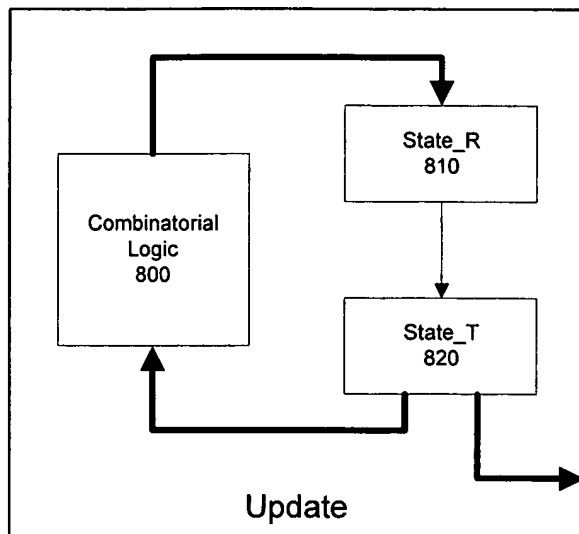
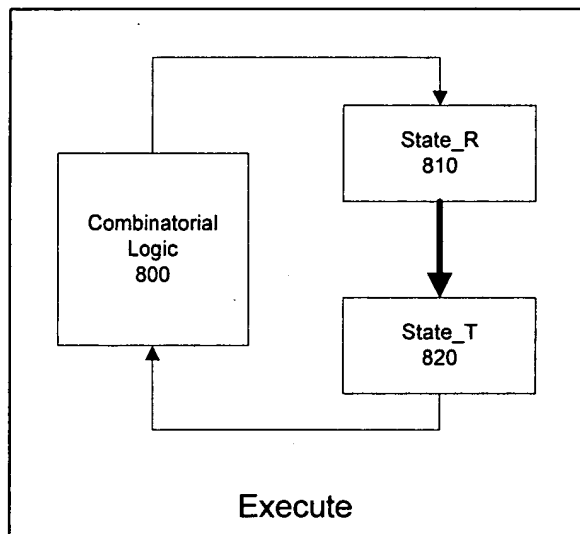


FIG. 8

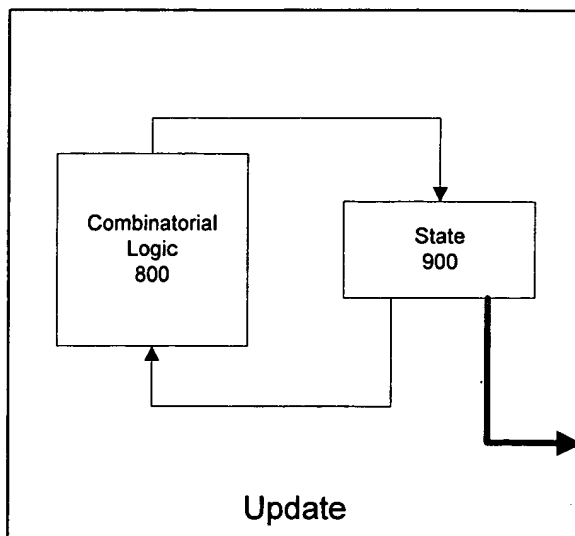
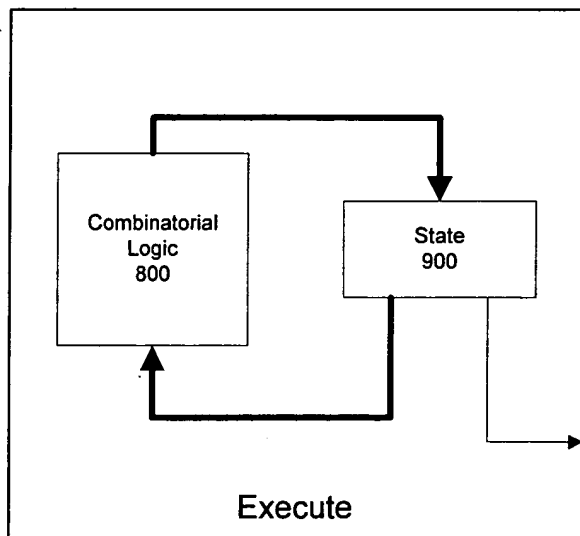


FIG. 9

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application
software
990

```
01010010011011001010101010100
1100101000101010010010101001010
1010000101101010110010010101001
0010110010100100110110010101010
1010100110010100010101001001010
1001010101000010110101011001001
0101001001011001010101010101010
1010010110010101010101010101010
0101000101010101101011001010101
```

002090-EE498560

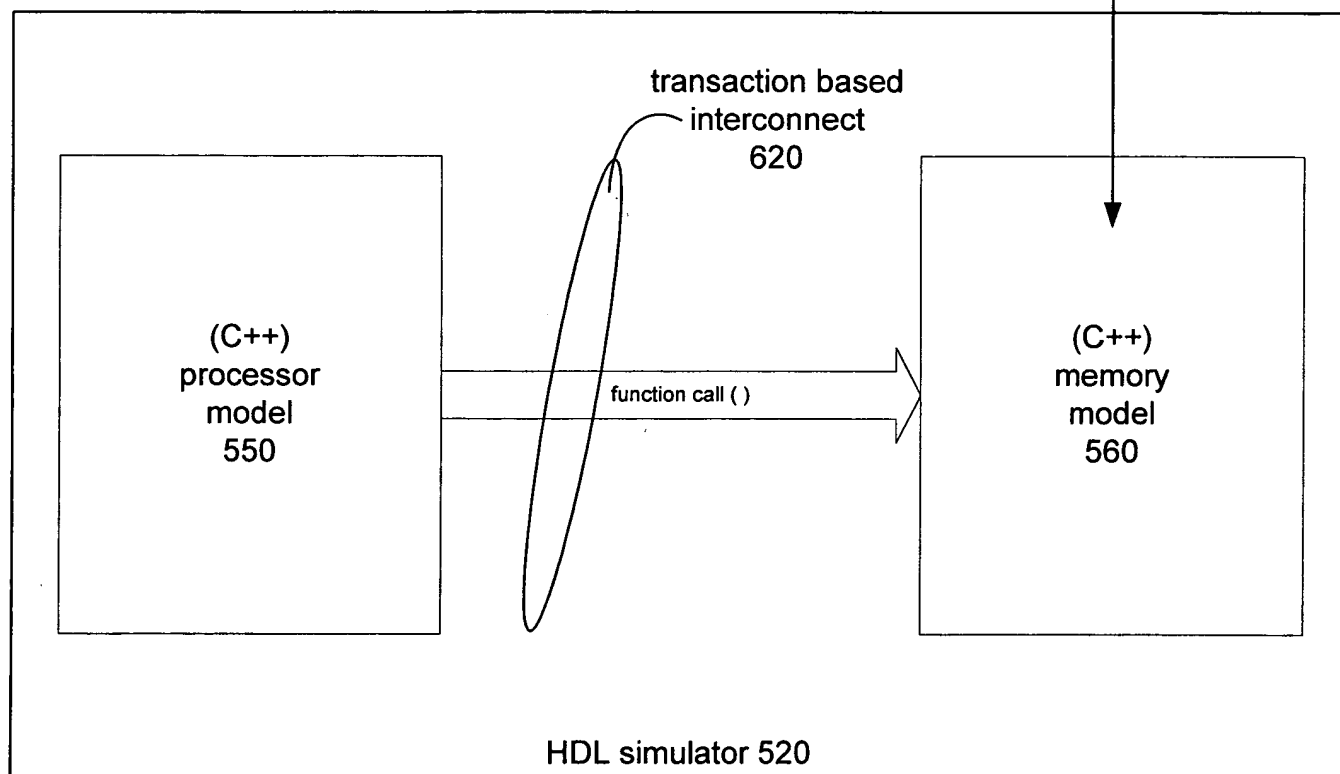


FIG. 10

The diagram illustrates the architecture of the HDL simulator 520. It features four primary functional blocks: a (c++) DSP model 910, a (VHDL) DSP model 920, a (c++) processor model 550, and a (c++) memory model 560. Each of these blocks is interfaced with a C++ / VHDL translator 510. The (c++) DSP model 910 and the (c++) processor model 550 are linked through a pin based interconnect 530, which is represented by four parallel bidirectional arrows. Similarly, the (c++) processor model 550 and the (c++) memory model 560 are connected via a transaction based interconnect 620, also shown with four parallel bidirectional arrows. The (c++) memory model 560 is further connected to an application software block 990. A data bus, depicted as a horizontal line with multiple vertical connections, spans the top of the diagram, linking the application software 990 to the (c++) memory model 560. A series of binary digits (0s and 1s) is shown along this bus, indicating data flow. The entire system is labeled as the HDL simulator 520.

FIG. 11

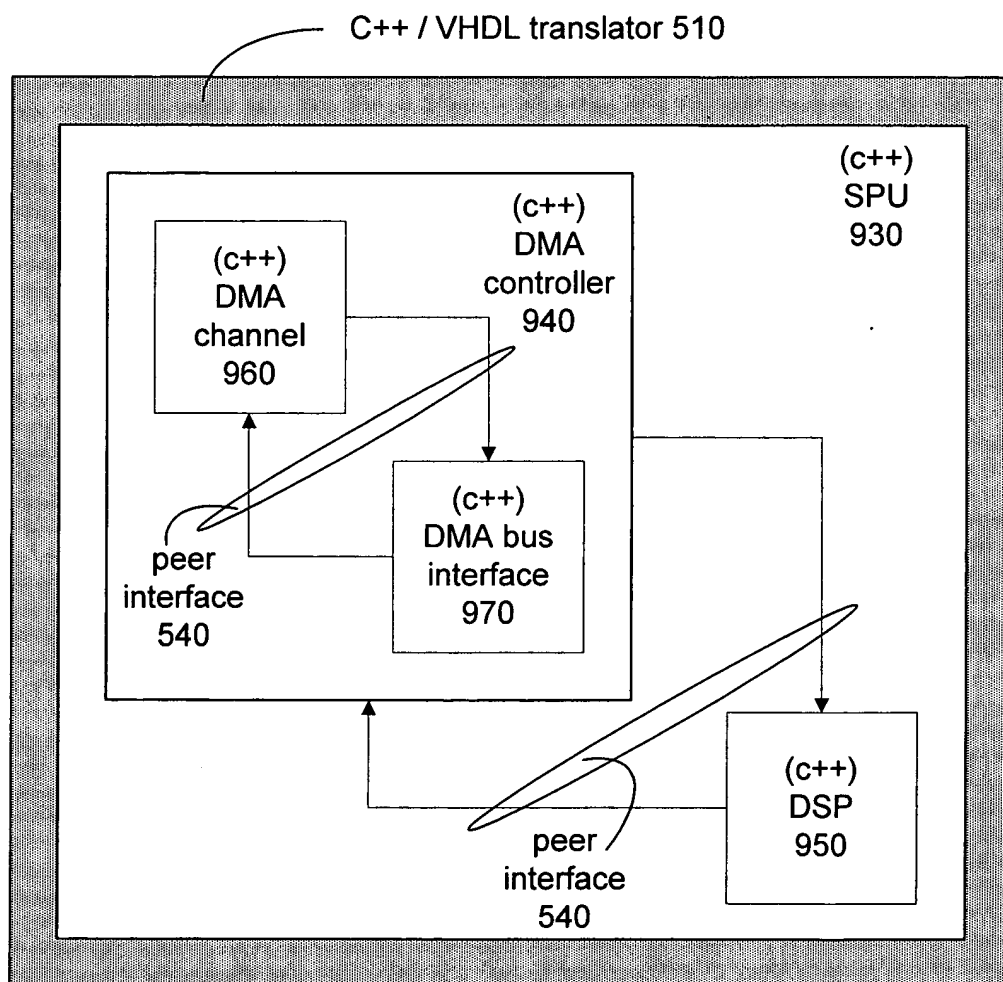


FIG. 12

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